FAIRCHILD SEMICONDUCTOR®

February 2008

MM74HCT14
Hex Inverting Schmitt Trigger

Features

- Typical propagation delay: 13ns
- Wide power supply range: 2V–6V
- Low quiescent current: 10μA maximum
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V
- TTL, LS pin-out and input threshold compatible

General Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

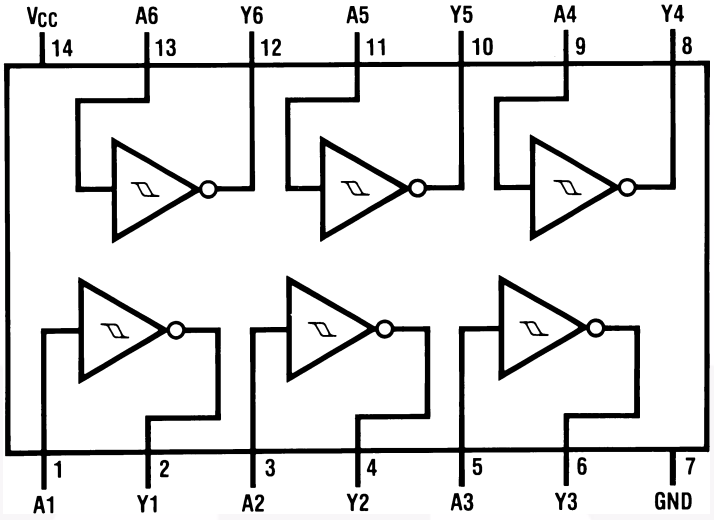
Order Number	Package Number	Package Description
MM74HCT14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

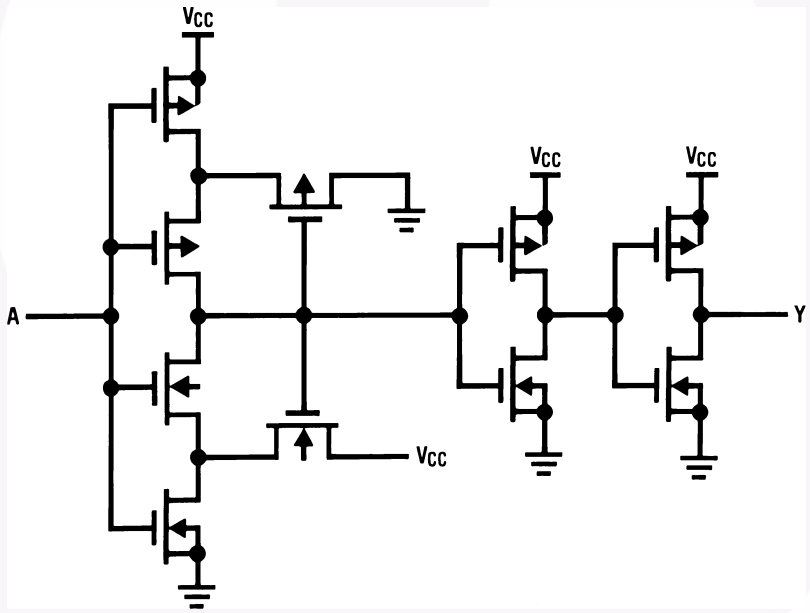
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Schematic Diagram



Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C

DC Electrical Characteristics[2]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$	$T_A = -40°C$ to 85°C		Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage	4.5	Minimum	1.5	1.2	1.2	V
		5.5		1.7	1.4	1.4	
		4.5	Maximum	1.5	1.9	1.9	
		5.5		1.7	2.1	2.1	
V_{T-}	Negative Going Threshold Voltage	4.5	Minimum	0.9	0.5	0.5	V
		5.5		1.0	0.6	0.6	
		4.5	Maximum	0.9	1.2	1.2	
		5.5		1.0	1.4	1.4	
V_H	Hysteresis Voltage	4.5	Minimum	0.6	0.4	0.4	V
		5.5		0.7	0.4	0.4	
		4.5	Maximum	0.6	1.4	1.4	
		5.5		0.7	1.5	1.5	
V_{OH}	Minimum HIGH Level Output Voltage		$V_{IN} = V_{IL}$, $\|I_{OUT}\| = 20\mu A$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
			$V_{IN} = V_{IL}$, $\|I_{OUT}\| = 4.0mA$, $V_{CC} = 4.5V$	4.2	3.98	3.84	
			$V_{IN} = V_{IL}$, $\|I_{OUT}\| = 4.8mA$, $V_{CC} = 5.5V$	5.2	4.98	4.98	
V_{OL}	Maximum LOW Level Voltage		$V_{IN} = V_{IH}$, $\|I_{OUT}\| = 20\mu A$	0	0.1	0.1	V
			$V_{IN} = V_{IH}$, $\|I_{OUT}\| = 4.0mA$, $V_{CC} = 4.5V$	0.2	0.26	0.33	
			$V_{IN} = V_{IH}$, $\|I_{OUT}\| = 4.8mA$, $V_{CC} = 5.5V$	0.2	0.26	0.33	
I_{IN}	Maximum Input Current		$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		1.0	10	μA
		5.5	$V_{IN} = 2.4V$ or $0.5V$[2]		2.4	2.4	mA

Note:

2. For a power supply of 5V ± 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15pF, $t_r = t_f$ = 6ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

V_{CC}= 5V ± 10%, C_L = 50pF, $t_r = t_f$ = 6ns (unless otherwise specified)

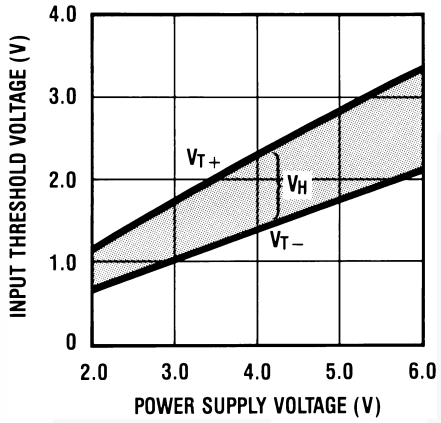
Symbol	Parameter	Conditions	T_A = 25°	T_A = –40°C to 85°C		Units
			Typ.	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay			20	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	ns
C_{PD}	Power Dissipation Capacitance(3)	(per gate)		25		pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

Note:

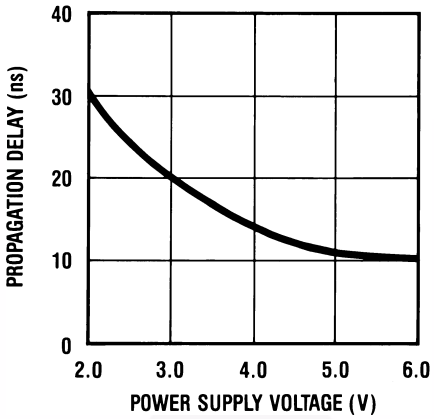
3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f+I_{CC}$.

Typical Performance Characteristics

Input Threshold, V_T+, V_T-, vs. Power Supply Voltage

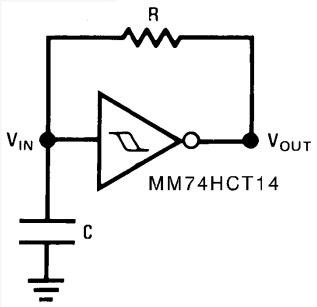


Propagation Delay vs. Power Supply



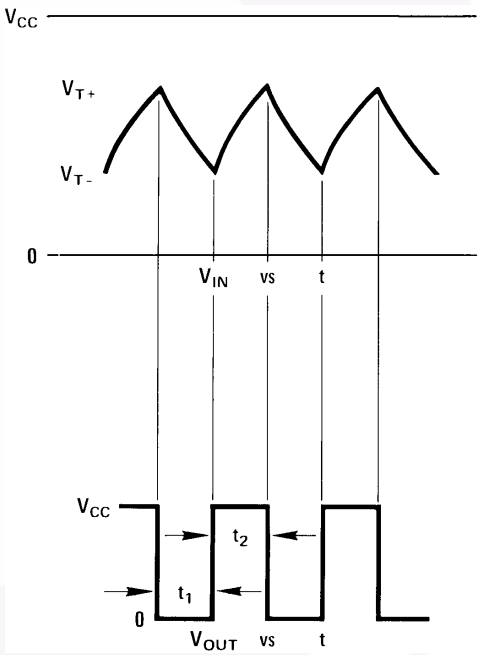
Typical Applications

Low Power Oscillator



$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$



Note:
The equations assume $t_1+t_2 >> t_{pd0}+t_{pd1}$

Physical Dimensions

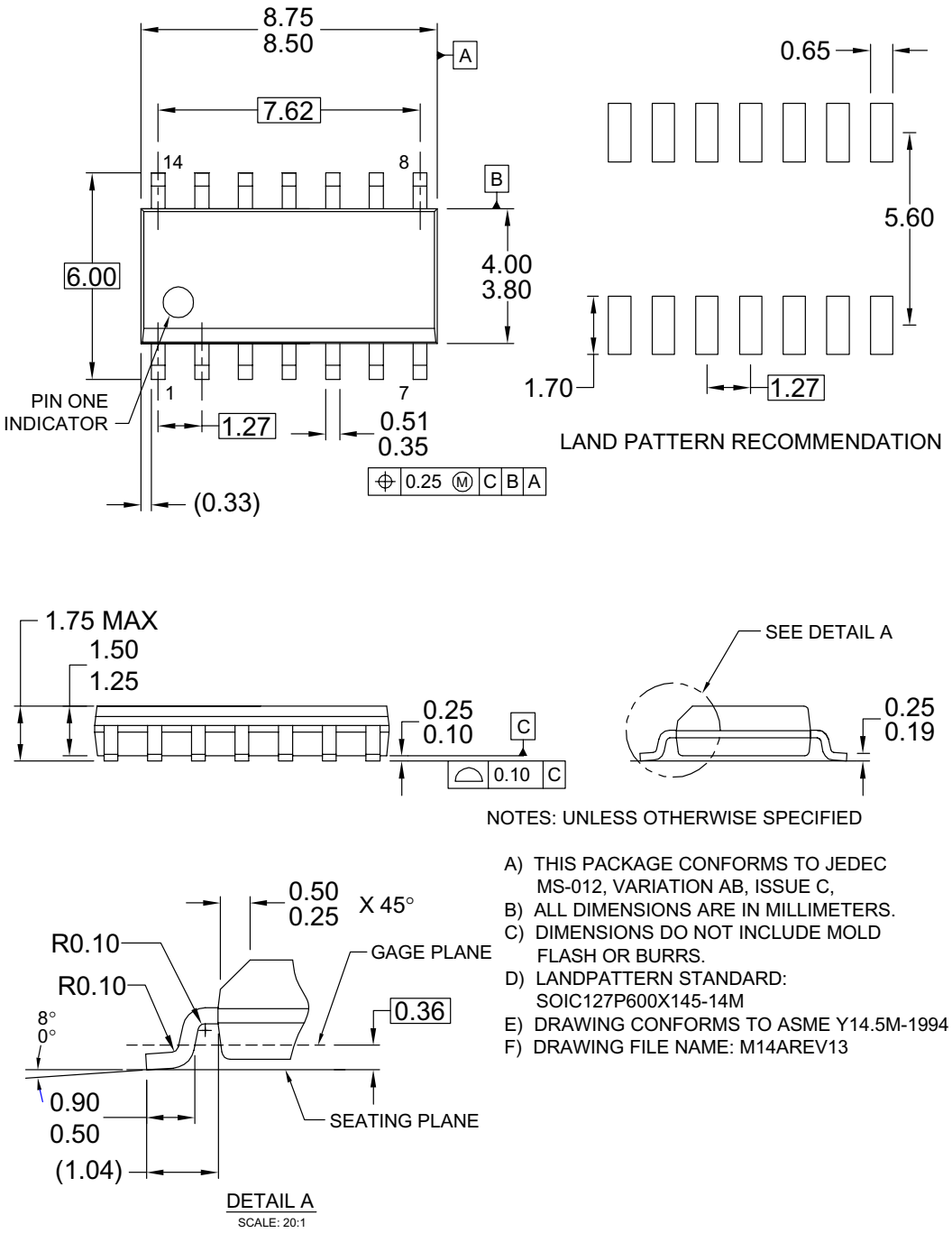


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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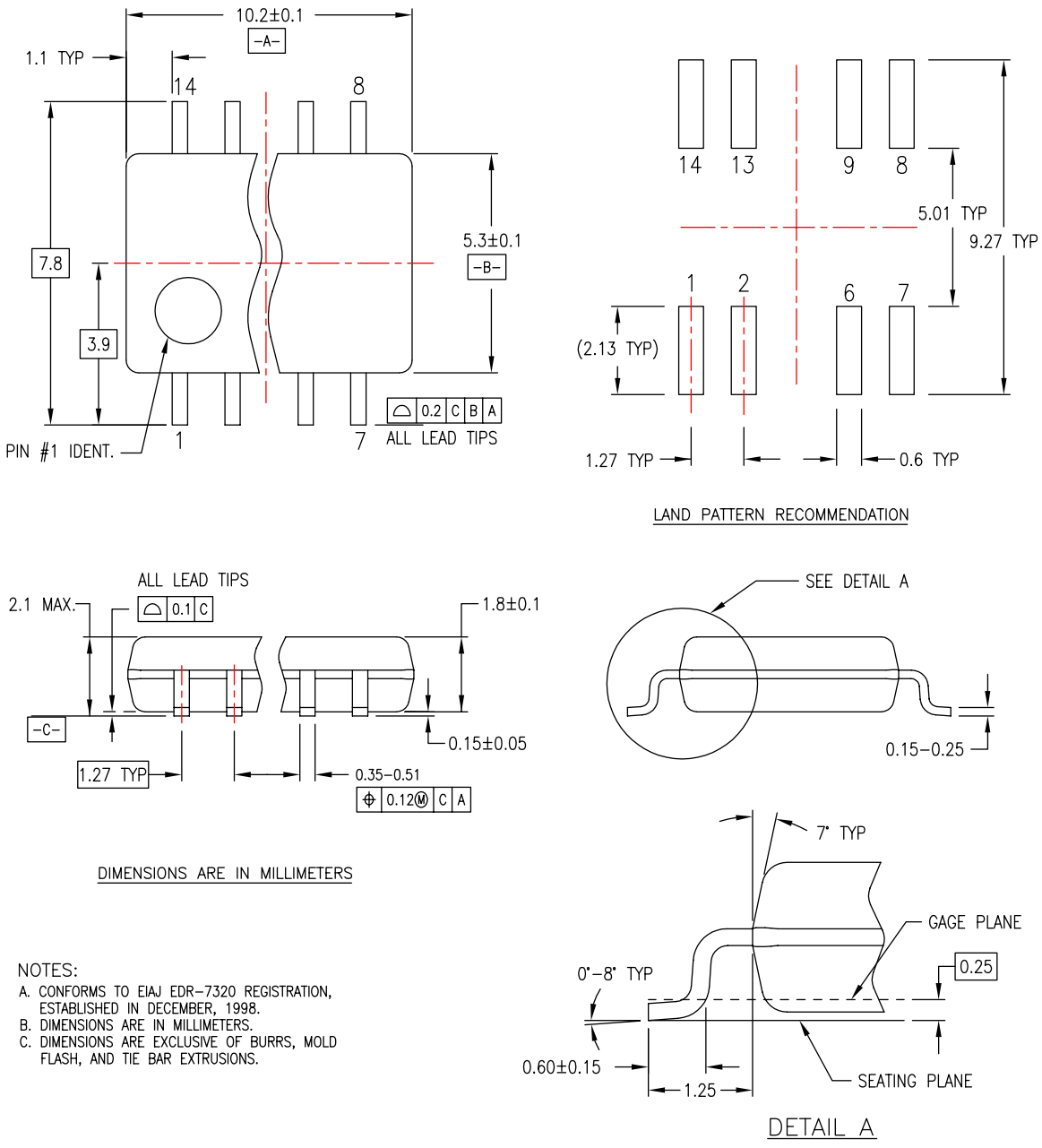
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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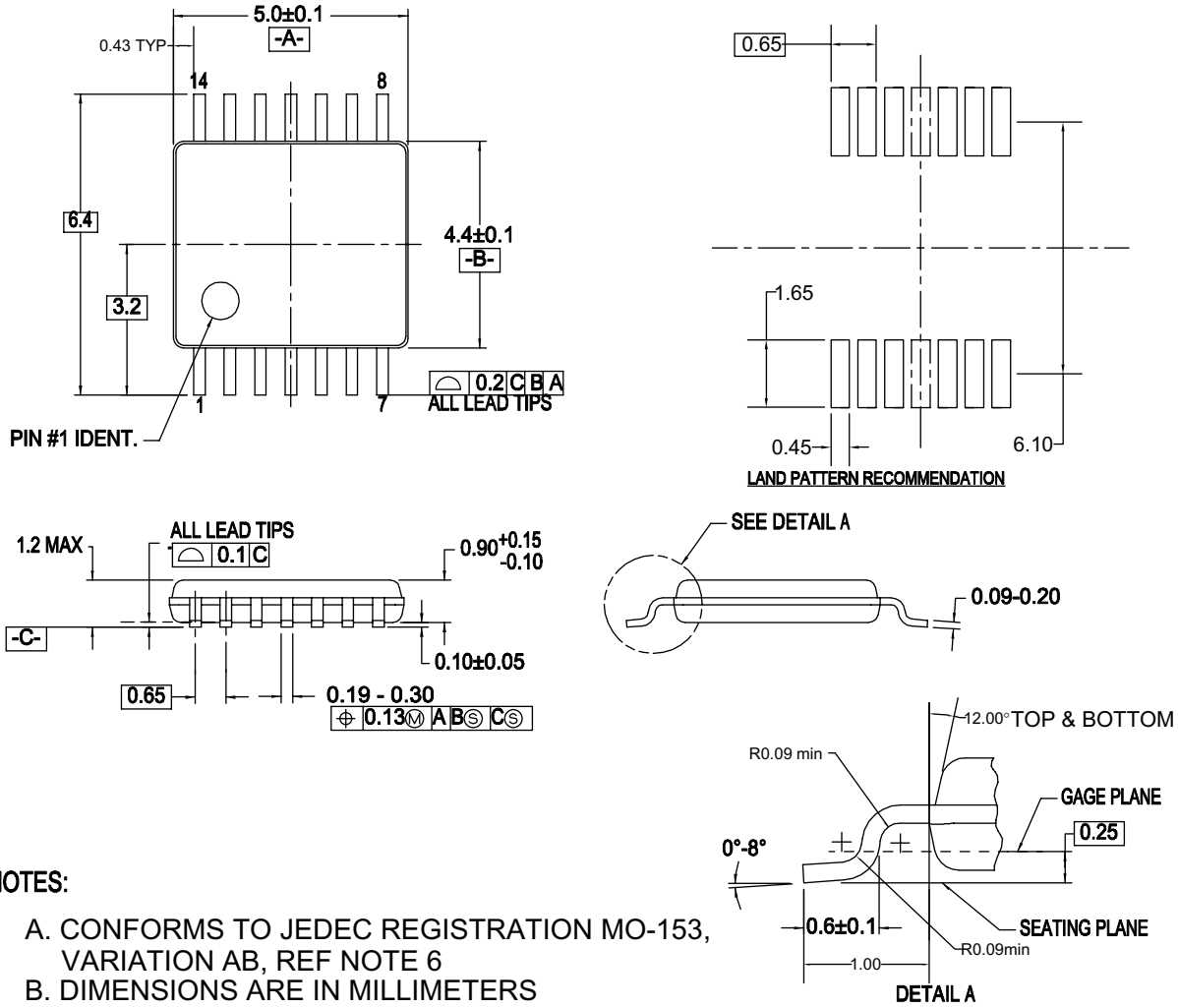
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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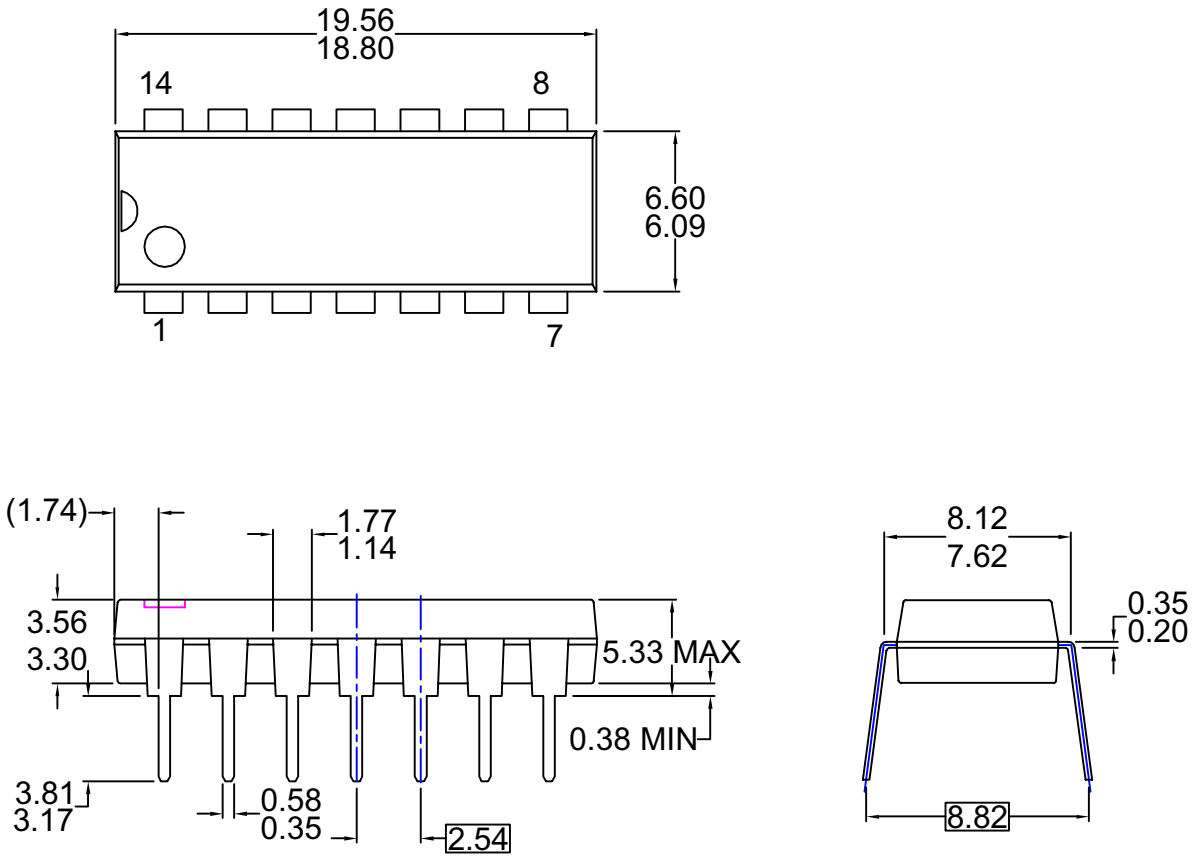
Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.
DIMENSIONS ARE EXCLUSIVE OF BURRS,

C) MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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